

FIGURE 1

parameter	meaning	typical value
$N$	number of input and output ports	64
$L$	number of input and output lines	512
$R$	number of lines per port	8
$K$	number of classes	8
$M$	number of scheduling modules	16
$S$	number of pipeline stages per scheduling module	1
$C$	number of cells per super-cell	8

FIGURE 2

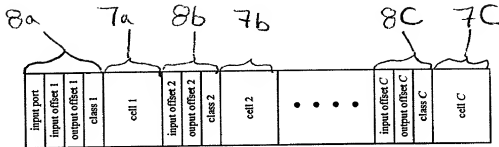


FIGURE 3

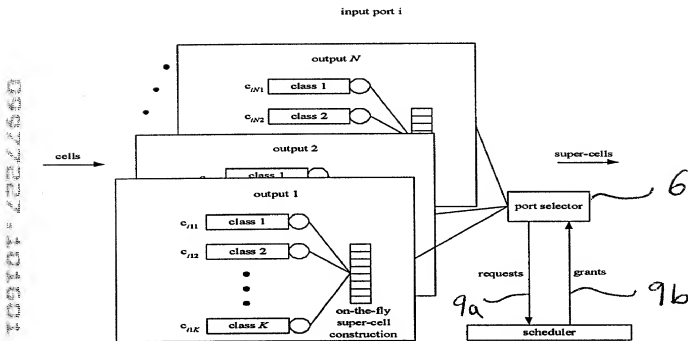


FIGURE 4

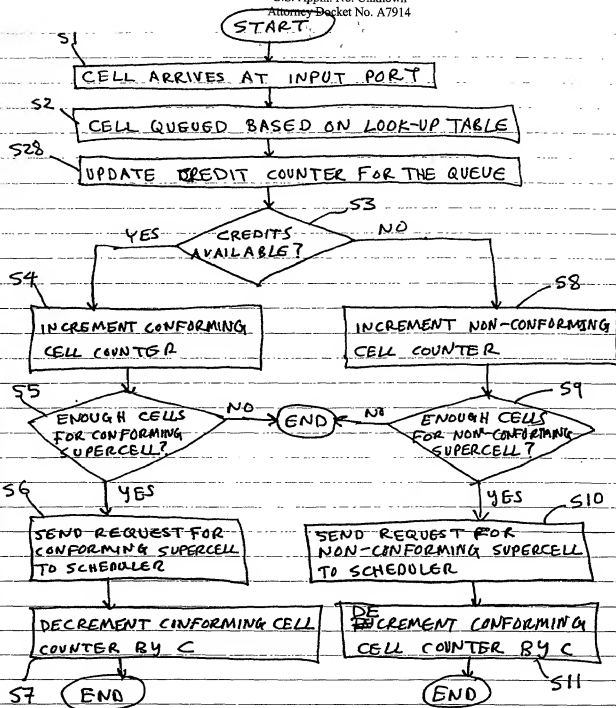


FIGURE 5(a)

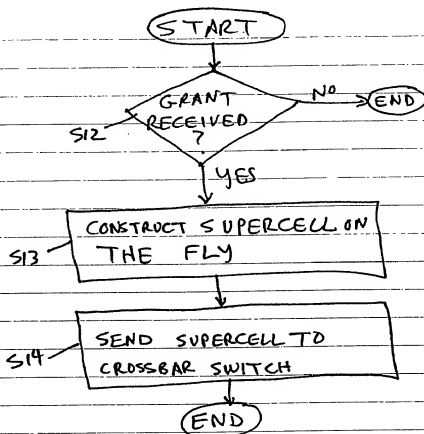


FIGURE 5(b)

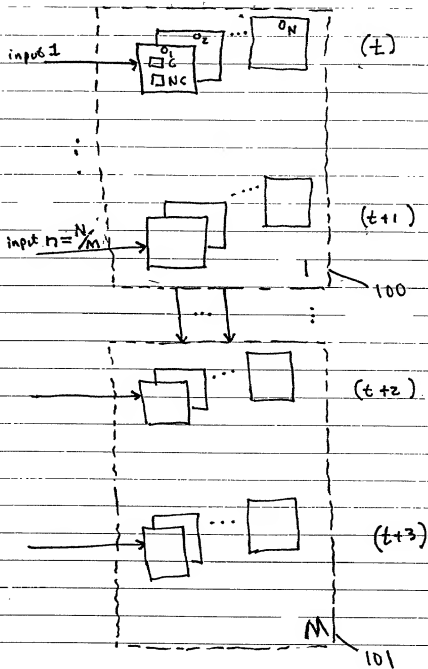


FIGURE 6

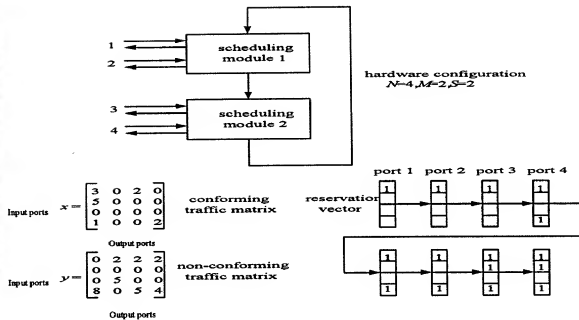


FIGURE 7

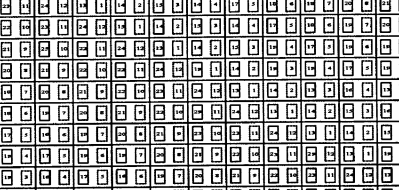
modules	m1		delay		m2		delay		m3		delay		m4		delay	
stages	s1	s2			s3	s4			s5	s6			s7	s8		
ports	p1 p2 p3 p4	p5 p6 p7 p8			p9 p10 p11 p12	p13 p14 p15 p16			p17 p18 p19 p20	p21 p22 p23 p24			p25 p26 p27 p28	p29 p30 p31 p32		
time slots																

FIGURE 8

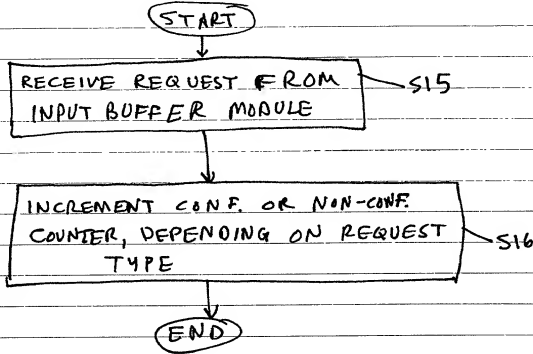


FIGURE 9

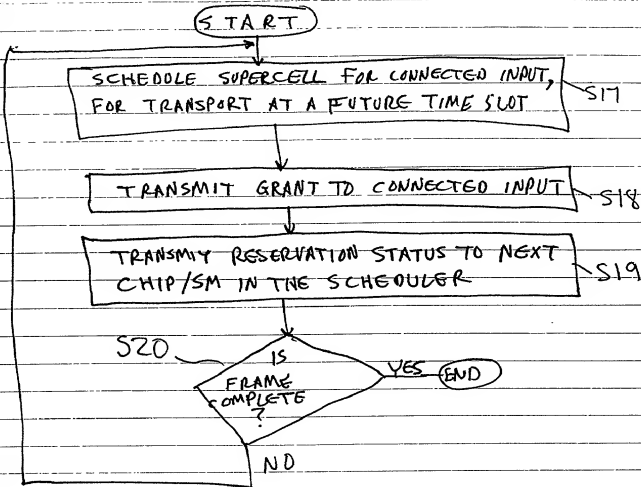


FIGURE 10

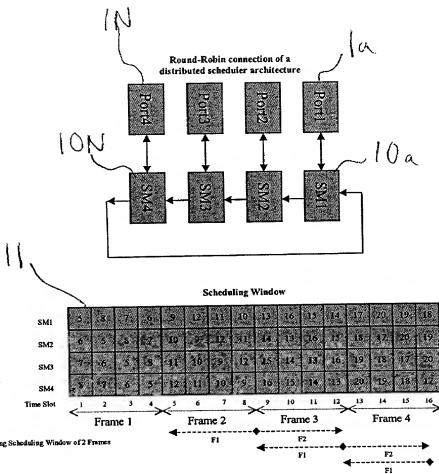


FIGURE 11

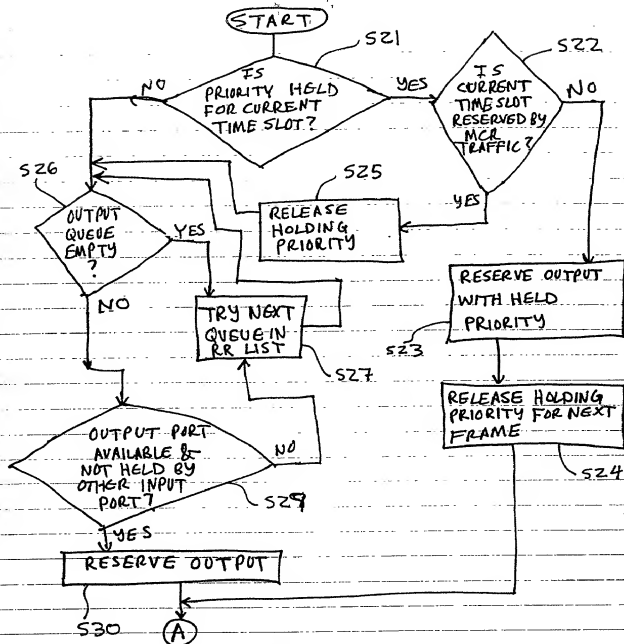


FIGURE 12 (a)

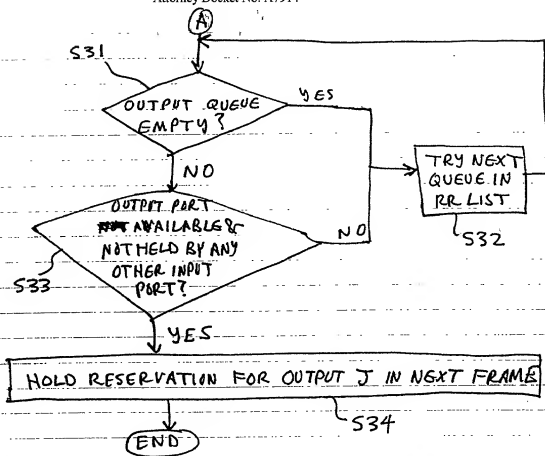


FIGURE 12C6)

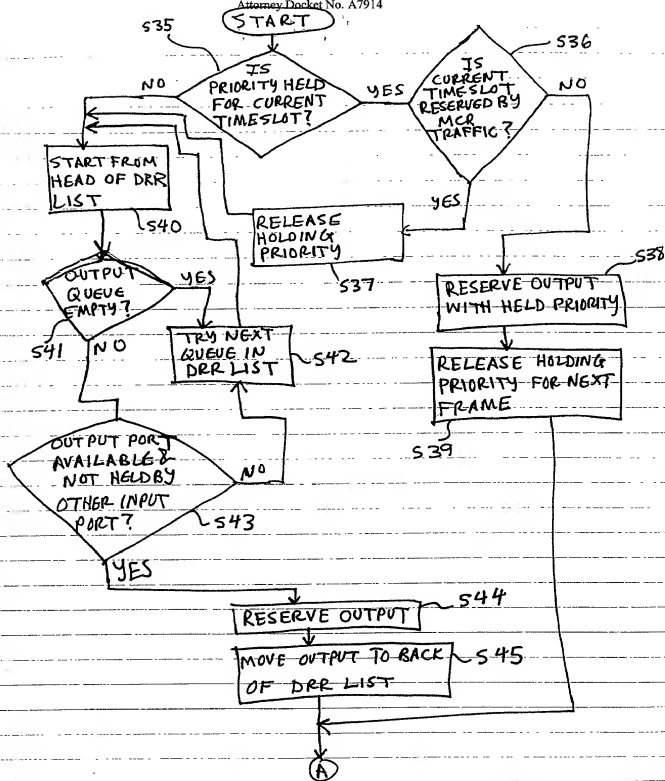


FIGURE 13(a)

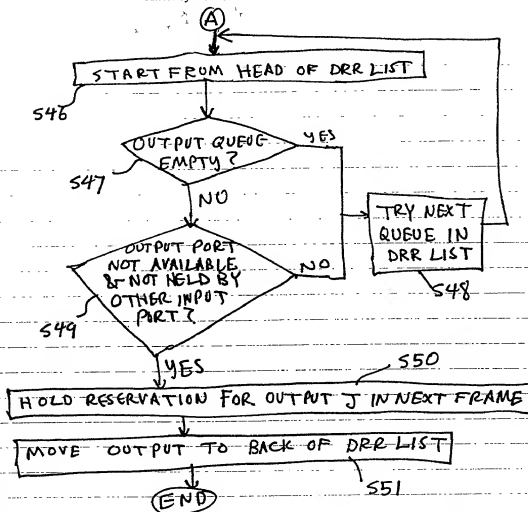


FIGURE 13 (b)

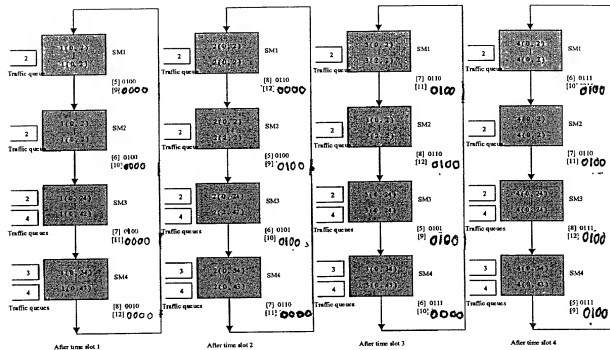


FIGURE 14(a)

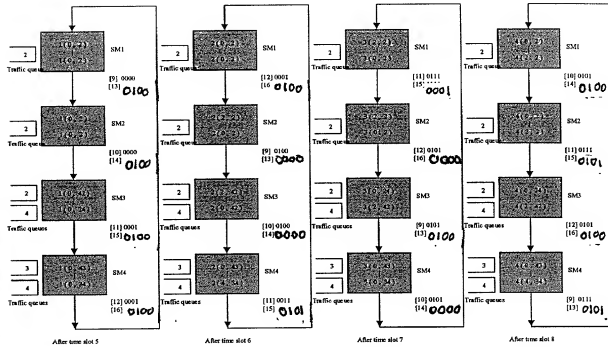


FIGURE 14(b)

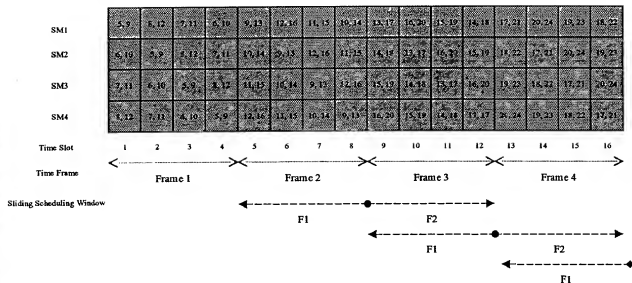


FIGURE 15

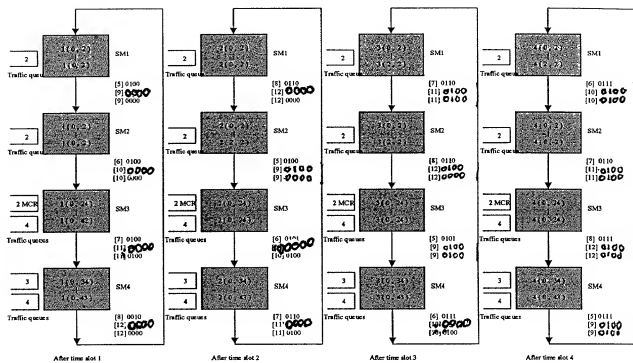


FIGURE 16

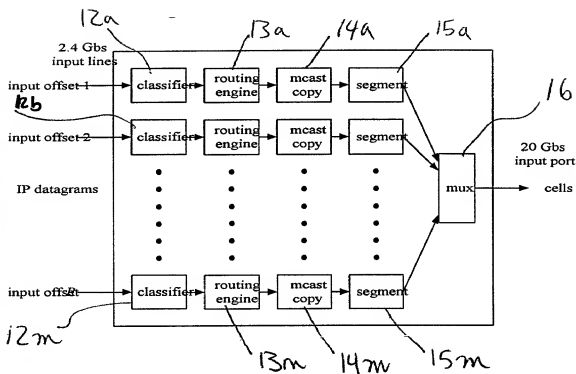


FIGURE 17

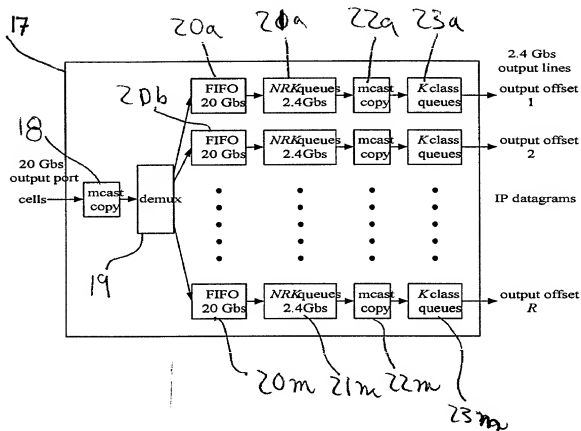


FIGURE 18